ABSTRACT

The present invention relates to the use of multiple store buffer forwarding in a microprocessor system with a restrictive memory model. In accordance with an embodiment of the present invention, the system and method allow load operations that are completely covered by two or more store operations to receive data via store buffer forwarding in such a manner as to retain the side effects of the restrictive memory model thereby increasing processor performance without violating the restrictive memory model. In accordance with an embodiment the present invention, a method for multiple store buffer forwarding in a system with a restrictive memory model includes executing multiple store instructions, executing a load instruction, determining that a memory region addressed by the load instruction matches a cacheline address in a memory, determining that data stored by the multiple store instructions completely covers the memory region addressed by the load instruction, and transmitting a store forward is OK signal.

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